UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,581	03/25/2004	Michael Karl Gschwind	AUS920030719US1	7129

45327 7590 08/24/2006

IBM CORPORATION (CS)
C/O CARR LLP
670 FOUNDERS SQUARE
900 JACKSON STREET
DALLAS, TX 75202

EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,581	GSCHWIND ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1, 2, 14, 21, 24 and 25 of U.S. Patent Application 10809579 contain every element of claims 1, 4, 12, 13, 29 and 30 of the instant application and as such provisionally anticipate claims 1, 4, 12, 13, 29 and 30 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of

obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objection

3. Claims 1-11, 16 and 22 are objected to because of the following informalities:

In claim 1, on line 11, the phrase "selected the memory blocks" should be replaced with "selected memory blocks of the plurality of memory blocks"; on line 9, "processing element" should be replace with "processing elements".

In claims 3-5, 9, 10 and 16, on line 1, it would be more appropriate to replace "where" with "wherein".

In claim 5, the phrase "one processing elements contains" contains typographical or grammatical errors.

In claim 10, on line 2, it would be more appropriate to replace "an on" with "one".

In claim 22, it would be more appropriate to replace "limiting" with "limited".

All dependent claims are objected to as having the same deficiencies as the claims they depend from. Appropriate correction is required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 29 and 30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Per claim 29, the claimed invention is a computer program product, which has a medium with a computer program. However, the computer program product itself is not stored in any tangible medium such as a hard disk or RAM.

Per claim 30, the computer program is not stored in any tangible medium.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claim teaches the processor comprising a microcode, a firmware, and a software code for processing coherence, where the specification does not provide any disclosure to support a **processor** comprising the above items. Appropriate correction is required.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 2, 3, 7, 17 and 24-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Per claim 2, the limitation "the system memory space" lacks sufficient antecedent basis.

Per claim 3, the limitation "the system memory hierarchy" lacks sufficient antecedent basis.

Per claim 7, the limitation "the processor" lacks sufficient antecedent basis.

Per claim 17, the limitation "at least one processing element" lacks sufficient antecedent basis.

Per claims 24-26, the limitation "the memory" lacks sufficient antecedent basis.

All dependent claims are rejected as having the same deficiencies as the claims they depend from. Appropriate correction is required.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-6, 8, 9-13, 15-18 and 20-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Patterson and Hennessy [Computer Architecture: A Quantitative Approach] (hereinafter "Patterson").

Per claim 1, Patterson teaches a processing system for providing a distributed ("directory entries can be distributed along with the memory", see page 679, paragraph 4) directory based coherence protocol utilizing an associated memory having a

coherence directory and associated directory data (see page 679-685, and Figs 8.22, 8.23, 8.24 and 8.25; memory and directory, see page 680, Fig.8.22), the associated memory further comprising:

a plurality of memory blocks each associated with different directory data (see page 679, paragraph 3);

a plurality of buffers interconnected to the memory (see caches, page 680, Fig.8.22);

a plurality of processing elements (see processors, page 680, Fig.8.22), each of the processing element coupled to different buffers of the plurality of buffers;

means for requesting selected the memory blocks from the memory;

means associated with the memory, responsive to the means for requesting for delivery, in response to the requesting, for delivery of a corresponding memory block of the memory blocks, a corresponding set of the coherence directory data from the memory, to an associated element of the processing elements (see the section Directory-Based Cache-Coherence Protocols: The Basis, pages 679-685);

means for the processing elements for detecting the delivery of the memory block, if the memory block of the processing element is available for a particular access mode, and if not, performing coherence actions correspond to the coherence directory data (the state transitions in Figs 8.24 and 8.25 and explanations paragraphs in page 683, 684 and 685 illustrate updating the directory to enforce coherency as accesses of difference access modes are requested. For instance page 685 describes when a block

is in Exclusive state, three possible coherence actions are performed when the coherence information is not compatible with the required access mode).

Per claim 2, Patterson further teaches the memory blocks are configured to provide the system memory space (the distributed shared memory form the system memory space of the system shown in page 680, Fig.8.22, see Distributed Shared Memory Architecture, pages 677-685).

Per claim 3, Patterson further teaches the memory blocks are used to provide a level of cache in the system memory hierarchy (memory blocks in cache/cache blocks, see page 679, paragraph 3).

Per claim 4, Patterson further teaches the processing elements are connected with the buffers connected to the memory via point to point links (each processor is connected to a cache via point to point link, see page 680, Fig.8.22).

Per claim 5, Patterson further teaches at least one processing elements contains at least a first processor, and at least one processing elements contain at least a second processor (see processors, page 680, Fig.8.22).

Per claim 6, Patterson further teaches the coherence is performed by the processing elements, said processing elements conveyed through said system via a physical coherence bus and a logical coherence bus, said busses further comprising:

multiple point-to-point linkages and multiple point-to-point coherence ring (between directories there are point to point links and any multiples of directories can form logical rings, see page 680, Fig.8.22);

unique signaling primitives, the unique signaling primitives signaling between nodes provided by the system and a messaging and signaling system provided in the memory (message sent between processors and directories, see page 681, Fig.8.23).

Per claim 8, Patterson further teaches memory requests resulting in coherence actions update directory information to at least one state not corresponding to an indication of one of resident, shared, and exclusive states (uncached state, see page 684, Fig.8.25; Invalid state, see page 683, Fig.8.24).

Per claim 9, Patterson further teaches processing elements causing such at least one state resolve them using protocol requests (resolving uncached state, see page 684, lines 7-11 and page 685, lines 1-3, also see Fig.8.25).

Per claim 10, Patterson further teaches that other processors detect the at least an on state and back off and retry at a later time, until the node having generated the at least one state, resolves the at least one state, by performing coherence actions and

updating the coherence directory (an uncached state indicates to other processors that the requested data is not present at the requested node, a Read Miss occurs; see page 684, lines 7-11 and pages 685, lines 1-3, also see Fig.8.25; coherence actions are performed to make the requested node the only sharing node, and other processors would retry the requests to the sharing node).

Per claim 11, Patterson further teaches the memory supports access to directory information by performing a read, write, and at least one Boolean operation on directory information (the bit vector values must be read, written, and compared/equaled in order to serve their function, see page 680, lines 4-11).

Per claim 12, Patterson teaches a method implementing a distributed ("directory entries can be distributed along with the memory", see page 679, paragraph 4) directory based coherence protocol (see page 679-685, and Figs 8.22, 8.23, 8.24 and 8.25), comprising:

requesting a memory block from a memory hierarchy level having a coherence directory and associated directory data (cache, memory and directory, see page 680, Fig.8.22),

generating a response including memory data and coherence information (messages sent among nodes to maintain coherence, see page 681 and Fig.8.23, the memory data request must also be serviced as well, see page 682, last paragraph) and updating directory information (tracking the state of each cache block and coherence

information related to processors sharing the blocks, see page 680; also see page 682, last paragraph),

receiving a response including memory data and coherence information from the memory hierarchy level (messages sent among nodes to maintain coherence, see page 681 and Fig.8.23, the memory data request must also be serviced as well, see page 682, last paragraph),

a step of performing coherence actions if the test indicates one of incompatibility or possible incompatibility (the state transitions in Figs 8.24 and 8.25 and explanations paragraphs in page 683, 684 and 685 illustrate updating the directory to enforce coherency as accesses of difference access modes are requested. For instance page 685 describes when a block is in Exclusive state, three possible coherence actions are performed when the coherence information is not compatible with the required access mode); and

a step of providing data a requestor of memory data (messages sent to satisfy the request, see page 682, last paragraph).

Per claim 13, Patterson further teaches that requests and responses are performed by sending and receiving data over logical point to point links (the messages and replied data values are sent between the processors and the directories, with a single source and a single destination, hence point-to point links; see page 681, lines 5-16 and Fig. 8.23).

Per claim 15, Patterson further teaches that the directory information includes a state indicating that at least one node is performing coherence actions as a result of receiving the response (state information provided under the columns "Processor", Coherence state of lock, and Bus/directory activity indicate the coherence actions are being performed with regard to directory information; see page 698, Fig.8.32).

Per claim 16, Patterson further teaches the step of performing coherence actions uses additional directory information to efficiently perform the coherence actions (request type information facilitate state transitions and maintain coherency, see page 683-685 and Figs.8.24 and 8.25).

Per claim 17, Patterson further teaches coherence actions are performed by at least one processing element by sending coherence requests to other processing elements (messages sent between processors, see page 681, paragraph 2, Fig.8.23 and page 682, last paragraph).

Per claim 18, Patterson further teaches those other processing elements are identified by additional information provided in the coherence directory (bit vector in directory, see page 680, lines 4-11).

Per claim 20, Patterson further teaches a response contains multiple data and coherence directory entries (see "write miss in shared state", page 685).

Per claim 21, Patterson further teaches the response is generated under the control of a tag array (bit vector, page 680, lines 4-11).

Per claim 22, Patterson further teaches the update of directory information is limiting to setting or resetting a plurality of bits, in response to the requesting step (bit vector values must be set and reset, see page 680, lines 4-11).

Per claims 23-26, it is clear the claims are already substantially described in claims 1, 4, 5, 11-13 and 17 as set forth above. Patterson's system shown in Page 680, Fig.8.22 is a symmetric multiprocessing system.

Per claim 27, Patterson further teaches the memory component also serves as signaling integration point, the memory component being the conduit for all signaling between processing elements (directory is distributed in memory as mentioned in claim 1, and all communication passes through the directory, see page 680, Fig.8.22; also there is no other signal path between processors other than those through the memory component).

Per claim 28, Patterson further teaches the memory component serves as physical integration point for building a symmetric multiprocessing system (the directory, which is distributed in memory as mentioned in claim 1, serves as a part of the central node controller, see page 680, Fig.8.22).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 7, 14, 19, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson and Hennessy [Computer Architecture: A Quantitative Approach] (hereinafter "Patterson").

Per claim 7, Patterson further teaches the processor additionally comprises a microcode (see examples of microcode shown in pages 696-699). Although Patterson does not specifically disclose a firmware or software code comprised in the processor for processing said coherence, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that complicated protocol algorithms such as the one described by Patterson in claims 1 and 12 should be implemented in software code for advantages such as more flexible adaptability and scalability, easier debugging and upgrading, and lesser cost of implementation over hardware implementation. It would have also been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that firmware provides the similar flexibility as software code as well as the characteristics of staying intact in the processor in the

absence of electrical power, and therefore can be used for processing said coherence while enjoying these advantages.

Per claim 14, Patterson further teaches the step of generating a response is performed atomically with respect to other generating and updating steps (see page 684, lines 3-5). Although Patterson does not specifically disclose that the step of updating directory information is also performed atomically, it does suggest it (some actions are atomic, see page 684, lines 3-5; implementing cache coherency using atomic operations, see page 695, paragraph to page 699). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to perform updating directory information atomically to avoid inconsistency in the shared data due to access conflicts and incoherency.

Per claim 19, Patterson further teaches the response containing memory data and coherence directory data is transmitted separately (see page 682, last paragraph), not in a single response. However, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to send the two pieces of data in a single response to reduce network traffic overhead and increase network throughput, as two separate responses would require at least two packets instead of the minimal of one packet for a single response.

Per claims 29 and 30, it is clear that the claims are already substantially described by claims 1 and 12 as set forth above. Although Patterson does not specifically disclose computer program product or compute code implementing the limitations, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that complicated protocol algorithms such as the one described by Patterson in claims 1 and 12 should be implemented as a program product including computer code for advantages such as more flexible adaptability and scalability, easier debugging and upgrading, and lesser cost of implementation over hardware implementation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

17 August 2006

Reginald A. Bragdon

REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100